


Features

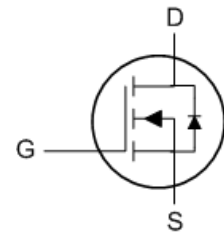
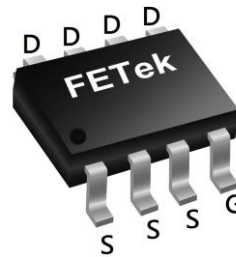
- Advanced Trench MOS Technology
- Low Gate Charge
- Low $R_{DS(ON)}$
- 100% EAS Guaranteed
- Green Device Available

Applications

- Power Management in Desktop Computer or DC/DC Converters.
- Isolated DC/DC Converters in Telecom and Industrial.

Product Summary

| BVDSS | RDSON | ID |
|-------|-------|-----|
| 30V | 8.0mΩ | 15A |

SOP8 Pin Configuration

Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|----------------------|--|------------|-------|
| V_{DS} | Drain-Source Voltage | 30 | V |
| V_{GS} | Gate-Source Voltage | ±20 | V |
| $I_D@T_A=25^\circ C$ | Continuous Drain Current ¹ | 15 | A |
| $I_D@T_A=70^\circ C$ | Continuous Drain Current ¹ | 12 | A |
| I_{DM} | Pulsed Drain Current ² | 60 | A |
| EAS | Single Pulse Avalanche Energy ³ | 39.2 | mJ |
| I_{AS} | Avalanche Current | 28 | A |
| $P_D@T_A=25^\circ C$ | Total Power Dissipation ⁴ | 3.1 | W |
| T_{STG} | Storage Temperature Range | -55 to 150 | °C |
| T_J | Operating Junction Temperature Range | -55 to 150 | °C |

Thermal Data

| Symbol | Parameter | Typ. | Max. | Unit |
|-----------------|--|------|------|------|
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient ¹ | --- | 75 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient ¹ , $t \leq 10\text{sec}$ | --- | 40 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case ¹ | --- | 24 | °C/W |

**N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------------|--|--|------|------|-----------|------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=250\mu A$ | 30 | --- | --- | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance ² | $V_{GS}=10V, I_D=12A$ | --- | 6.0 | 8 | m Ω |
| | | $V_{GS}=4.5V, I_D=12A$ | --- | 9.4 | 11 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}=V_{DS}, I_D=250\mu A$ | 1.2 | 1.7 | 2.2 | V |
| I_{DSS} | Drain-Source Leakage Current | $V_{DS}=30V, V_{GS}=0V, T_J=25^\circ\text{C}$ | --- | --- | 1 | μA |
| | | $V_{DS}=30V, V_{GS}=0V, T_J=55^\circ\text{C}$ | --- | --- | 5 | |
| I_{GSS} | Gate-Source Leakage Current | $V_{GS}=\pm 20V, V_{DS}=0V$ | --- | --- | ± 100 | nA |
| g_{fs} | Forward Transconductance | $V_{DS}=5V, I_D=12A$ | --- | 55 | --- | S |
| R_g | Gate Resistance | $V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$ | 0.8 | 1.7 | 2.6 | Ω |
| Q_g | Total Gate Charge (4.5V) | $V_{DS}=15V, V_{GS}=10V, I_D=12A$ | --- | 7.1 | --- | nC |
| Q_{gs} | Gate-Source Charge | | --- | 2.2 | --- | |
| Q_{gd} | Gate-Drain Charge | | --- | 3.1 | --- | |
| $T_{d(on)}$ | Turn-On Delay Time | $V_{DD}=15V, V_{GS}=10V, R_G=3\Omega$ $I_D=12A$ | --- | 7 | --- | ns |
| T_r | Rise Time | | --- | 18.8 | --- | |
| $T_{d(off)}$ | Turn-Off Delay Time | | --- | 19.5 | --- | |
| T_f | Fall Time | | --- | 3.4 | --- | |
| C_{iss} | Input Capacitance | $V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$ | --- | 693 | --- | pF |
| C_{oss} | Output Capacitance | | --- | 332 | --- | |
| C_{rss} | Reverse Transfer Capacitance | | --- | 34 | --- | |

Diode Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------|--|---|------|------|------|------|
| I_S | Continuous Source Current ^{1,5} | $V_G=V_D=0V$, Force Current | --- | --- | 12 | A |
| V_{SD} | Diode Forward Voltage ² | $V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$ | --- | --- | 1 | V |

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=28A$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

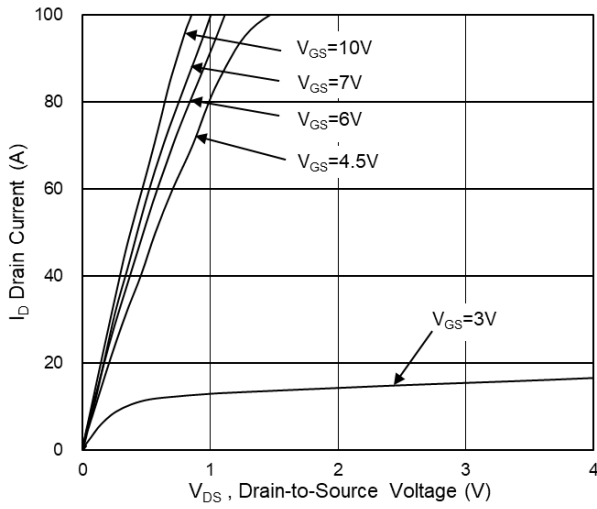


Fig.1 Typical Output Characteristics

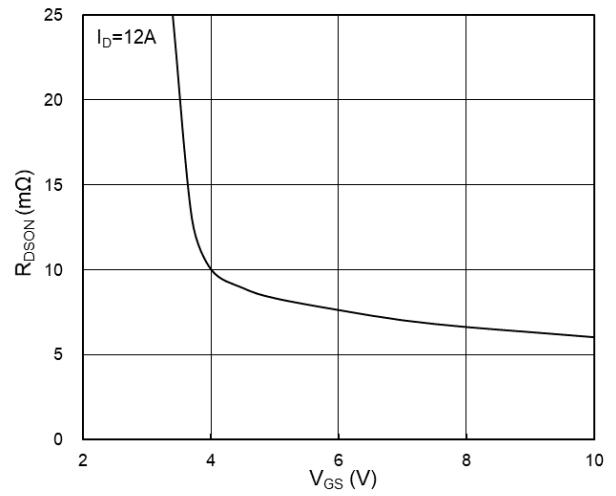


Fig.2 On-Resistance vs G-S Voltage

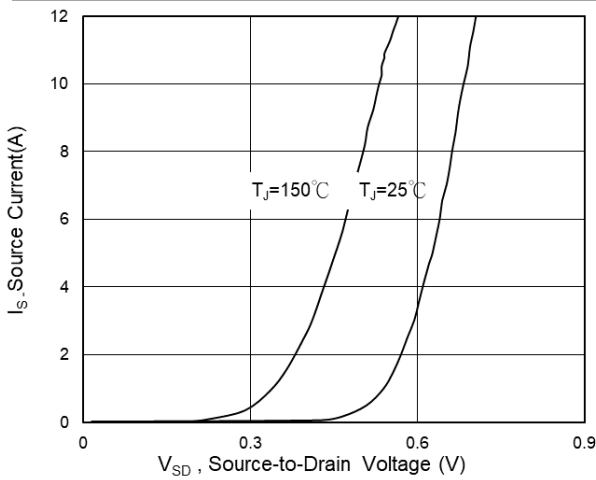


Fig.3 Source Drain Forward Characteristics

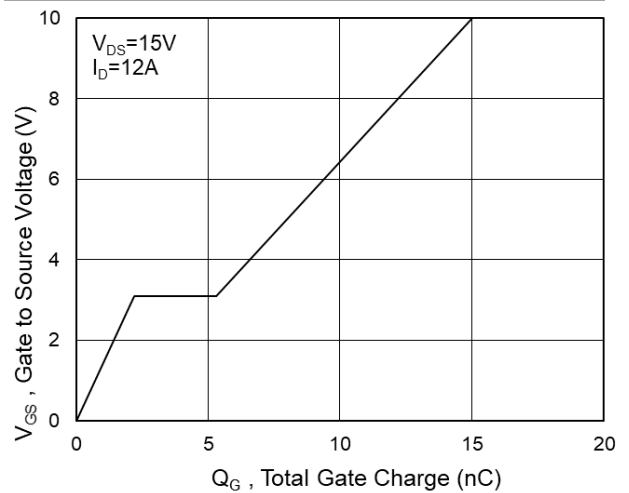


Fig.4 Gate-Charge Characteristics

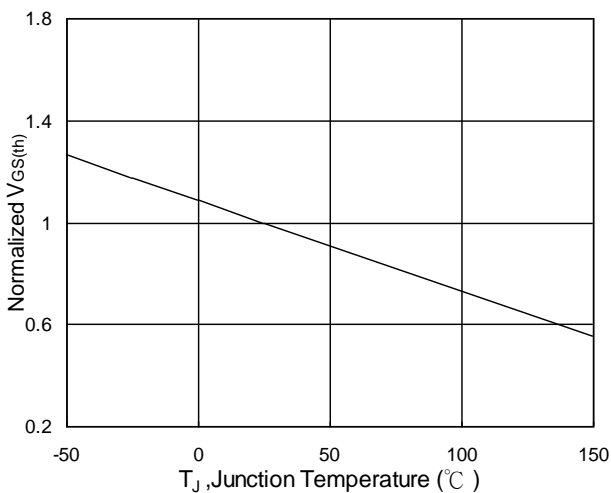


Fig.5 Normalized $V_{GS(th)}$ vs T_J

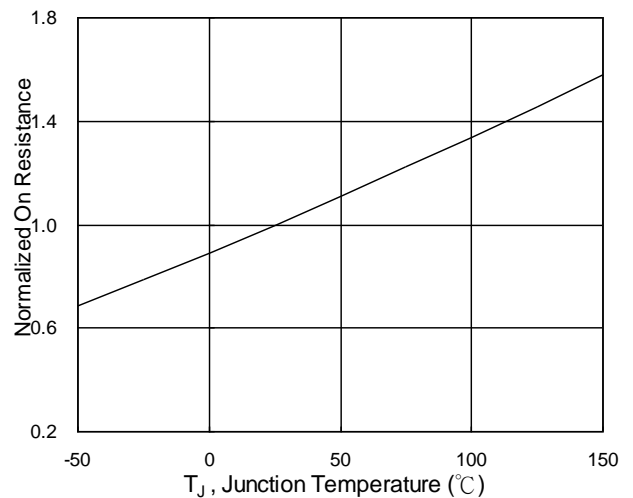


Fig.6 Normalized R_{DSON} vs T_J

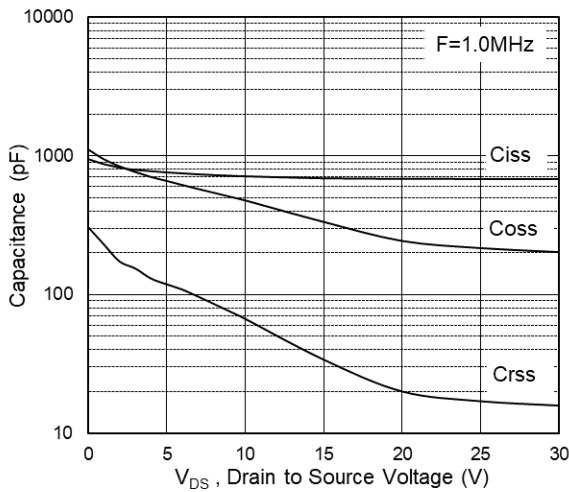


Fig.7 Capacitance

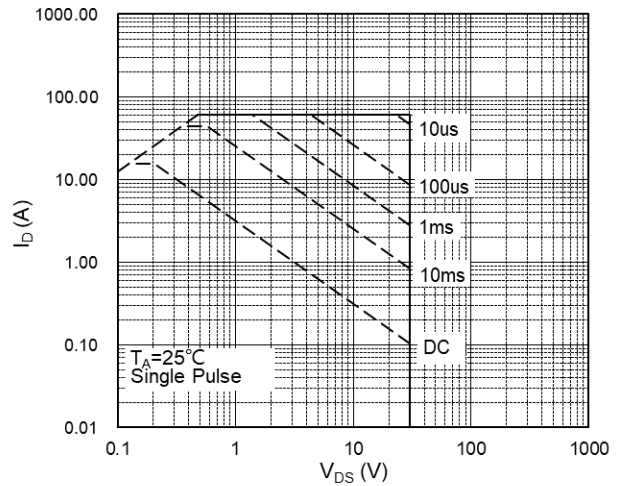


Fig.8 Safe Operating Area

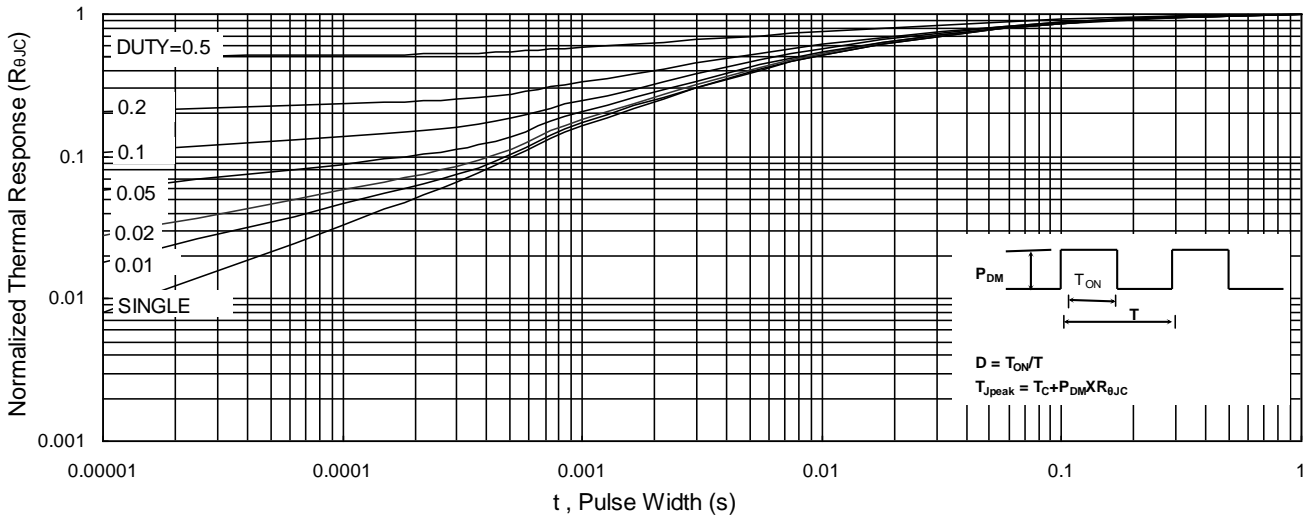


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform

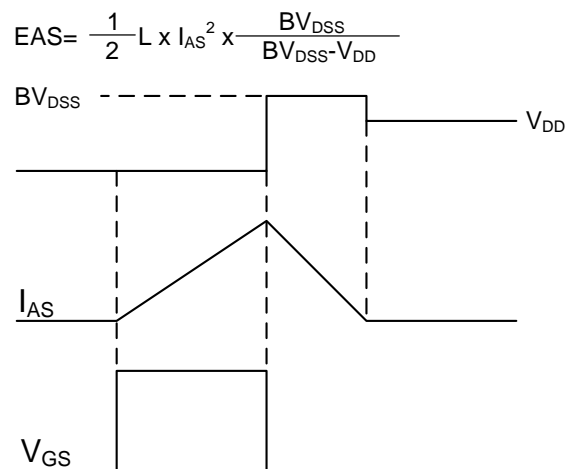


Fig.11 Unclamped Inductive Switching Waveform