

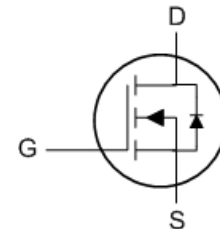
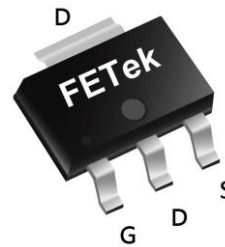
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

**Product Summary**


BVDSS	RDSON	ID
100V	100mΩ	3.3A

**Description**

The FKL0034 is the high cell density trenched N-ch MOSFETs, which provides excellent RDSON and efficiency for most of the small power switching and load switch applications. The FKL0034 meets the RoHS and Green Product requirement with full function reliability approved.

**SOT223 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	±20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.3	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	2.2	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	12	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation <sup>3</sup>	2.2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	---	55	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	12	°C/W

**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.3A	---	75	100	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2.7A	---	85	120	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	2	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =3.3A	---	8	---	S
Q <sub>g</sub>	Total Gate Charge (10V)	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>D</sub> =3.3A	---	11.9	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	2.8	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	1.7	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =50V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω I <sub>D</sub> =2A	---	3.8	---	ns
T <sub>r</sub>	Rise Time		---	25.8	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	16	---	
T <sub>f</sub>	Fall Time		---	8.8	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	450	---	pF
C <sub>oss</sub>	Output Capacitance		---	55	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	16	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	2.5	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =2A, dI/dt=100A/μs, T <sub>J</sub> =25°C	---	35	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	17	---	nC

Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
3. The power dissipation is limited by 150°C junction temperature
4. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

Typical Characteristics

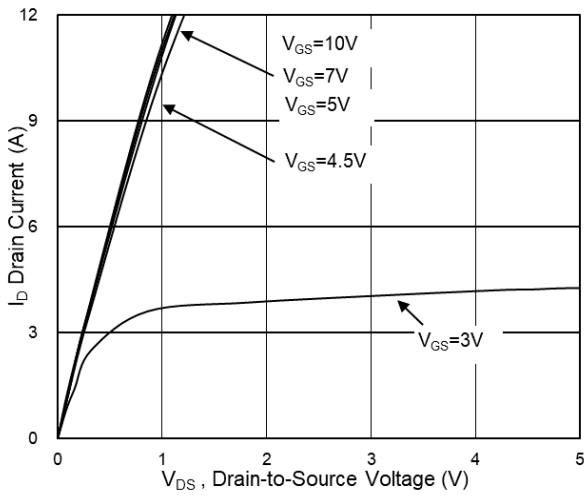


Fig.1 Typical Output Characteristics

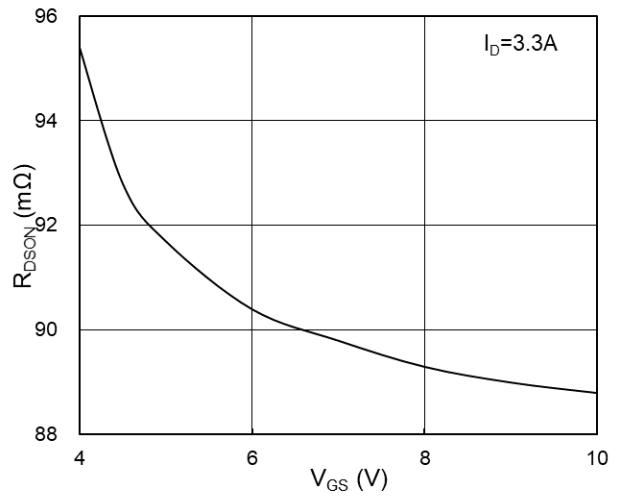


Fig.2 On-Resistance vs. G-S Voltage

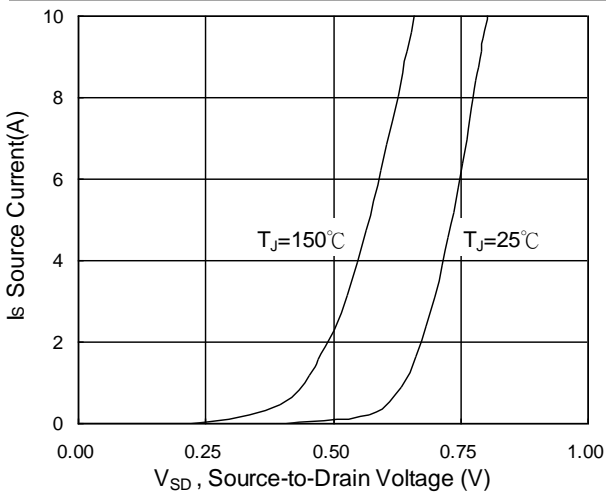


Fig.3 Source Drain Forward Characteristics

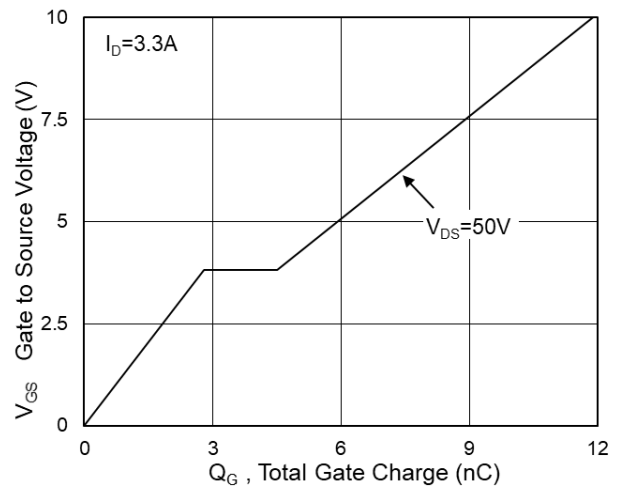


Fig.4 Gate-Charge Characteristics

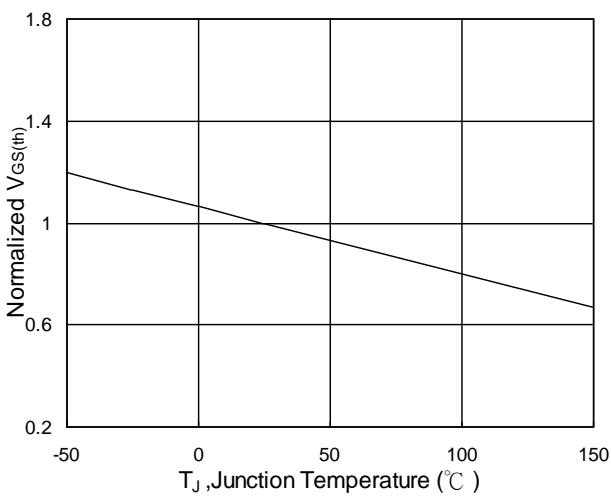


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

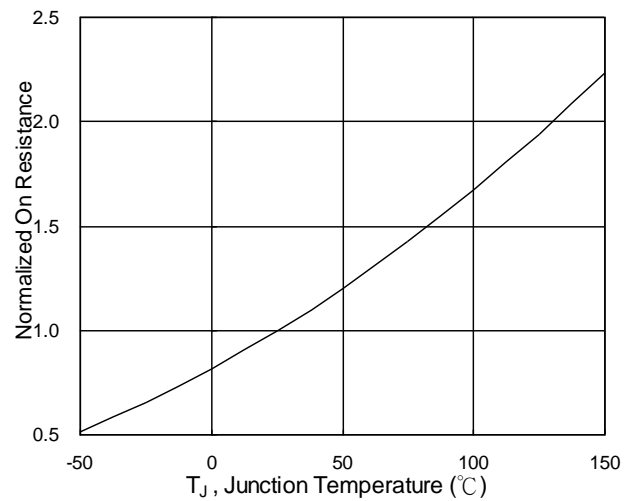


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$

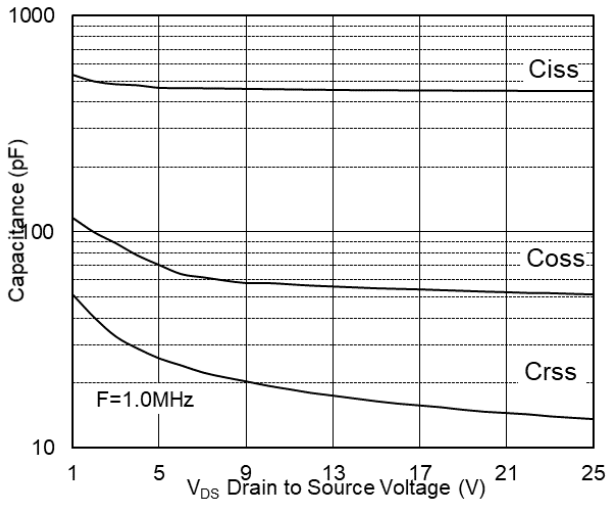


Fig.7 Capacitance

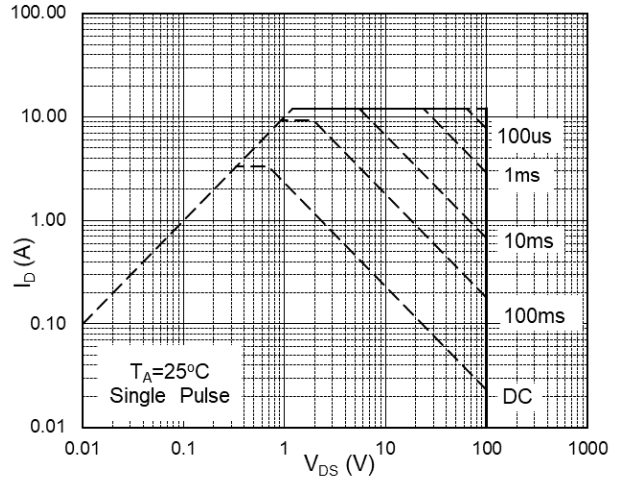


Fig.8 Safe Operating Area

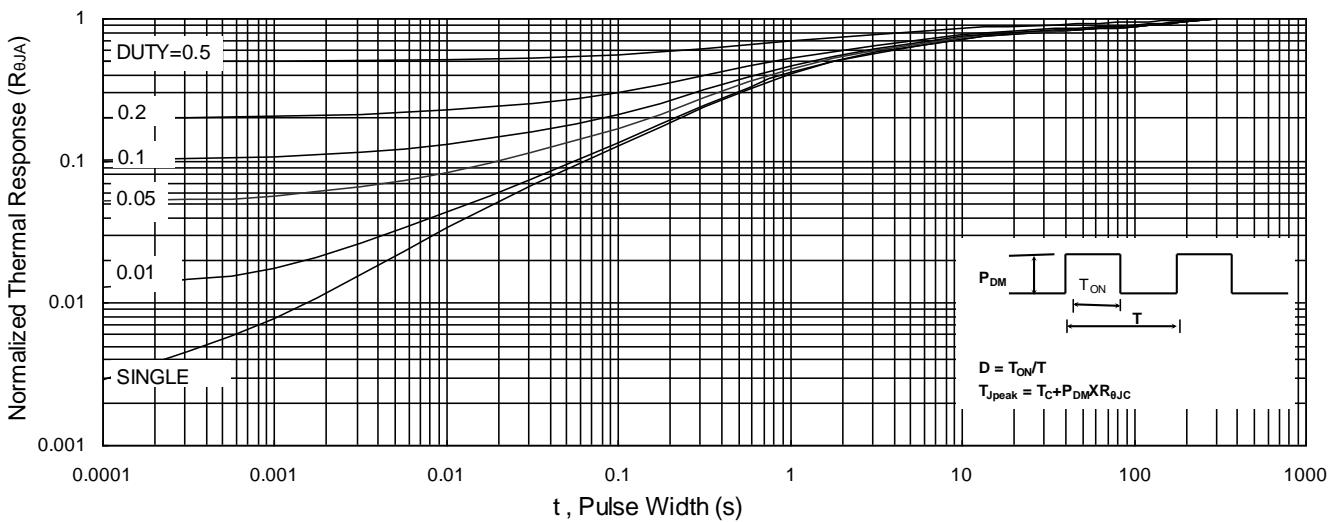


Fig.9 Normalized Maximum Transient Thermal Impedance

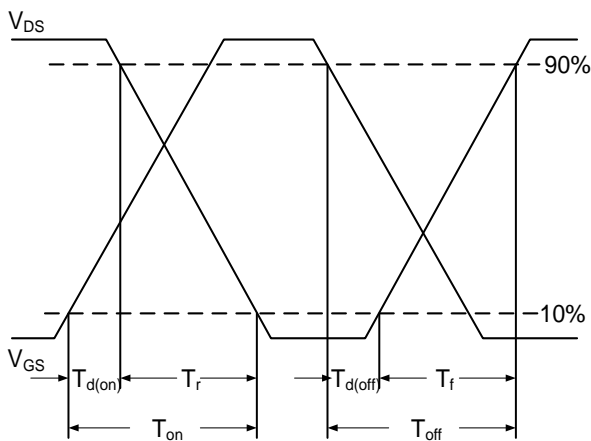


Fig.10 Switching Time Waveform

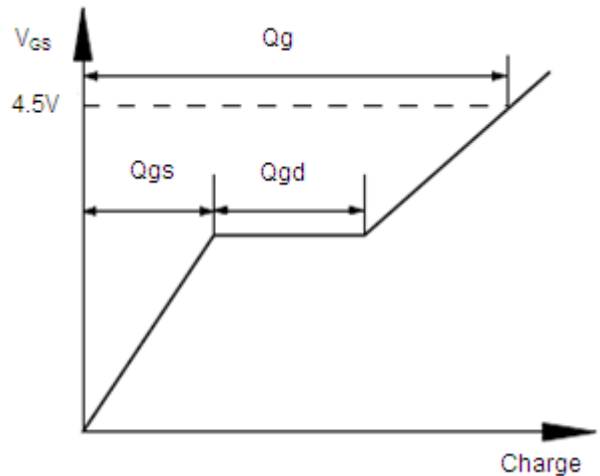
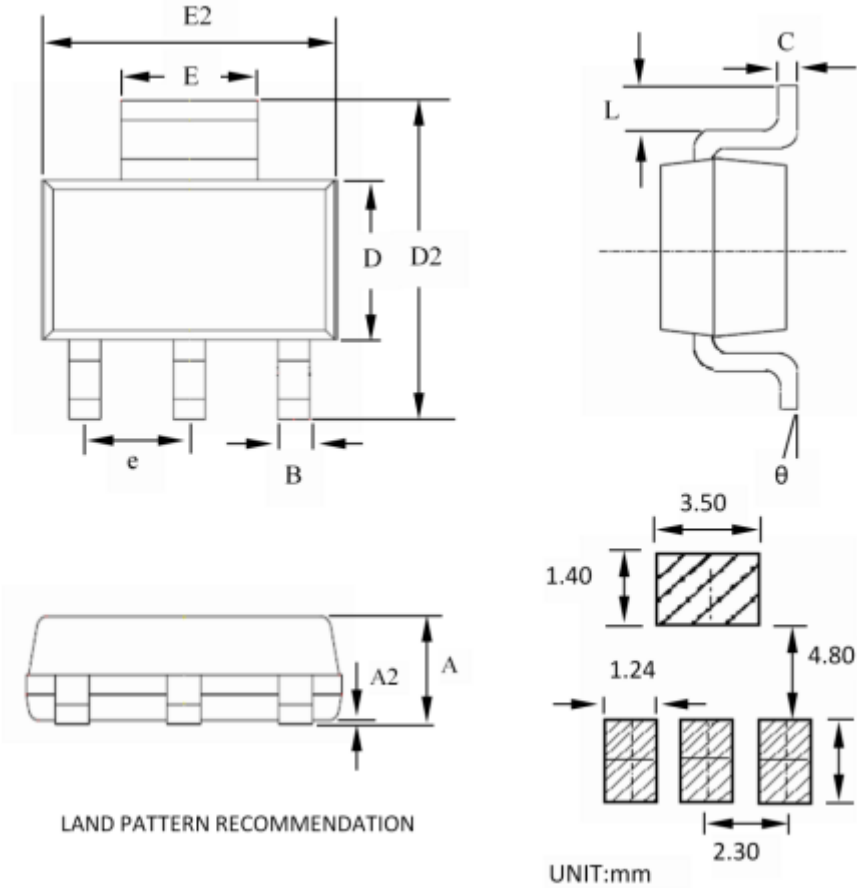


Fig.11 Gate Charge Waveform

# SOT223 Package Outline Dimensions



SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	--	1.80	0.059	--	0.071
A2	0.02	--	0.10	0.001	--	0.004
B	0.60	0.70	0.84	0.024	0.028	0.033
C	0.23	--	0.35	0.009	--	0.014
D	3.30	3.50	3.70	0.130	0.138	0.146
D2	6.70	--	7.30	0.264	--	0.287
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	6.30	6.50	6.70	0.248	0.256	0.264
L	0.75	0.90	1.00	0.030	0.035	0.039
θ	0°	--	10°	0°	--	10°
e	--	2.30	--	--	0.091	--