



- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

## Product Summary



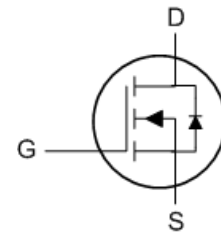
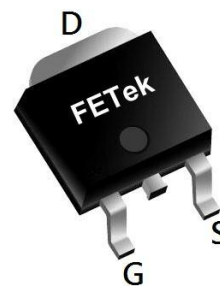
BVDSS	RDSON	ID
75V	12mΩ	62A

## Description

The FKD8016 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKD8016 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

## TO252 Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	75	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current <sup>1</sup>	62	A
$I_D@T_C=70^\circ\text{C}$	Continuous Drain Current <sup>1</sup>	49	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	200	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	80	mJ
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	89	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	1.3	$^\circ\text{C/W}$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	75	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=10A$	---	9.6	12	m $\Omega$
		$V_{GS}=4.5V, I_D=8A$	---	12	14.5	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=64V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=64V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	32	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	0.66	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=64V, V_{GS}=10V, I_D=4A$	---	60.9	---	nC
$Q_{gs}$	Gate-Source Charge		---	8.1	---	
$Q_{gd}$	Gate-Drain Charge		---	17.9	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=40V, V_{GS}=10V, R_G=3.3\Omega, I_D=4A$	---	12.2	---	ns
$T_r$	Rise Time		---	24.5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	50.5	---	
$T_f$	Fall Time		---	17.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=50V, V_{GS}=0V, f=1\text{MHz}$	---	3120	---	$\mu F$
$C_{oss}$	Output Capacitance		---	140	---	
$C_{rss}$	Reverse Transfer Capacitance		---	110	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	62	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=4A, dI/dt=100A/\mu s$ ,	---	18.6	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	65	---	nC

## Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is  $V_{DD}=50V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=40A$
4. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

Typical Characteristics

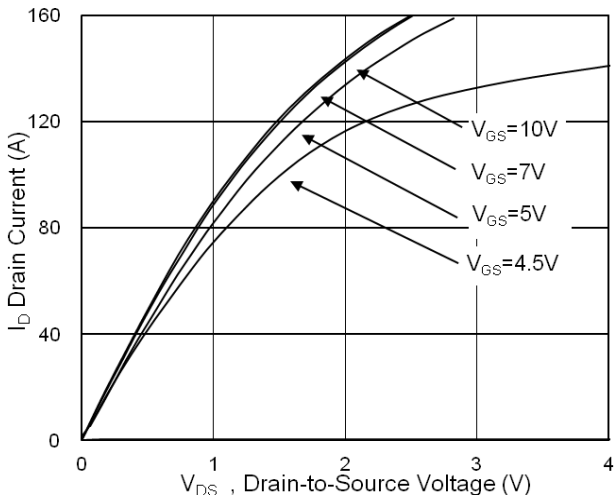


Fig.1 Typical Output Characteristics

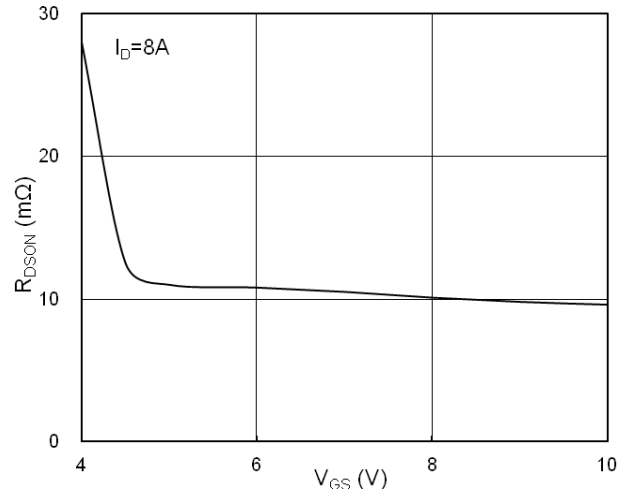


Fig.2 On-Resistance vs G-S Voltage

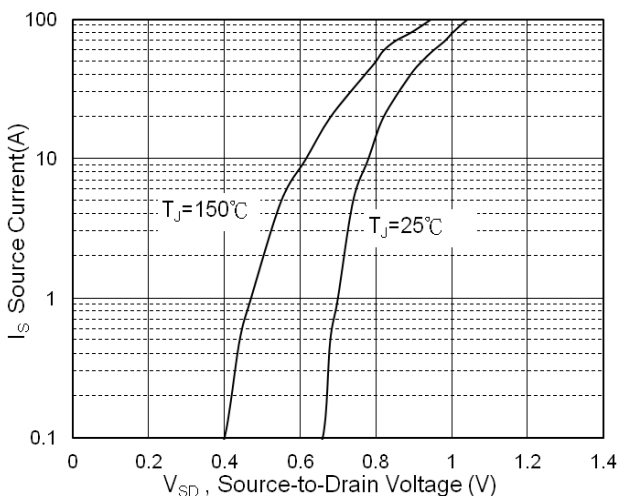


Fig.3 Source Drain Forward Characteristics

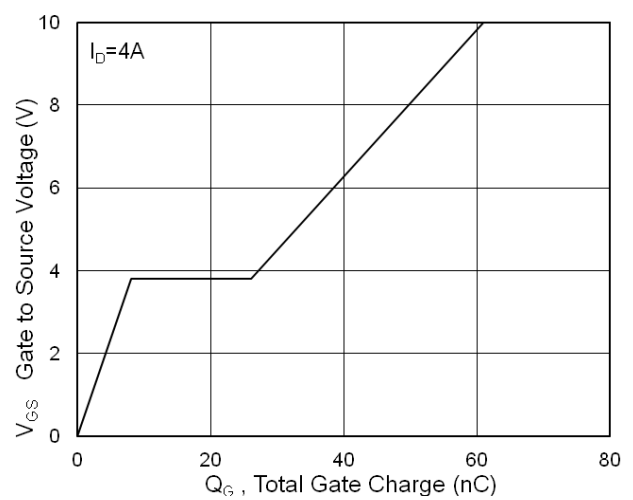


Fig.4 Gate-Charge Characteristics

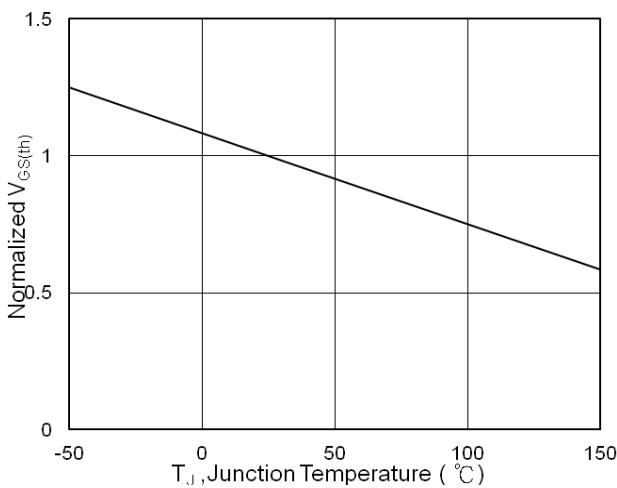


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

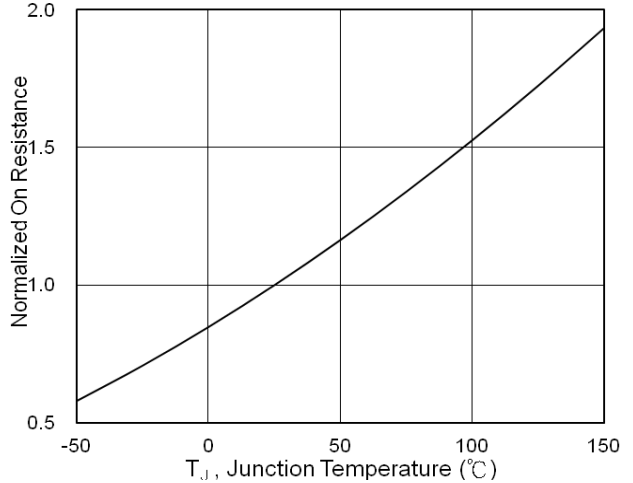


Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$

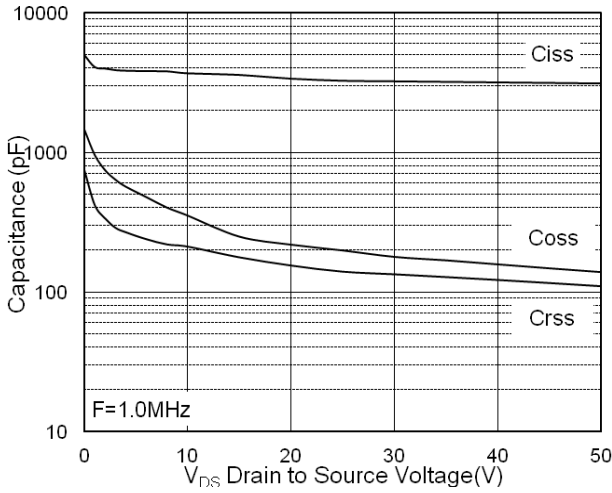


Fig.7 Capacitance

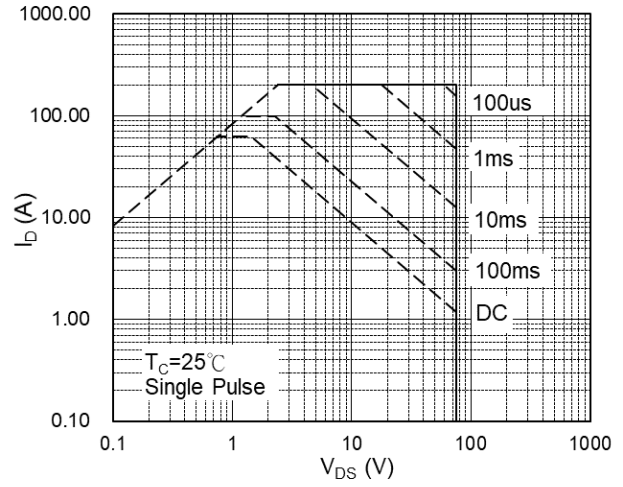


Fig.8 Safe Operating Area

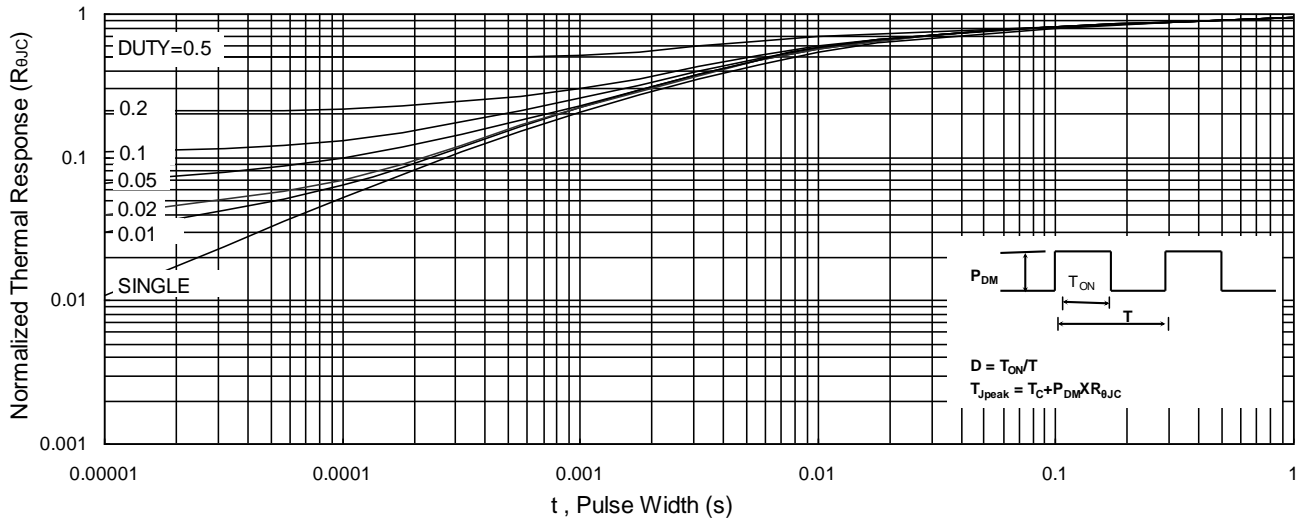


Fig.9 Normalized Maximum Transient Thermal Impedance



Fig.10 Switching Time Waveform



Fig.11 Unclamped Inductive Switching Waveform