

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

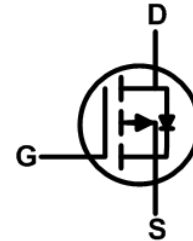
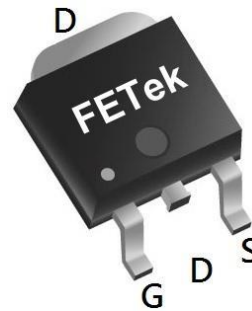
Product Summary


BVDSS	RDSON	ID
-40V	65mΩ	-16A

Description

The FKD4101 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKD4101 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ -10V ¹	-16	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, V_{GS} @ -10V ¹	-10	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, V_{GS} @ -10V ¹	-4.5	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, V_{GS} @ -10V ¹	-3.6	A
I_{DM}	Pulsed Drain Current ²	-32	A
EAS	Single Pulse Avalanche Energy ³	21	mJ
I_{AS}	Avalanche Current	-20.5	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	25	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	5	$^\circ C/W$

**Electrical Characteristics (T_J=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-40	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.015	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-8A	---	---	65	mΩ
		V _{GS} =-4.5V, I _D =-4A	---	---	100	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	---	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	3.52	---	V/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-32V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-32V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-10A	---	6	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-8A	---	5.8	---	nC
Q _{gs}	Gate-Source Charge		---	1.2	---	
Q _{gd}	Gate-Drain Charge		---	2.1	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-12V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	13.2	---	ns
T _r	Rise Time		---	8	---	
T _{d(off)}	Turn-Off Delay Time		---	40	---	
T _f	Fall Time		---	3.5	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	620	---	pF
C _{oss}	Output Capacitance		---	69	---	
C _{rss}	Reverse Transfer Capacitance		---	52	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,5}	V _G =V _D =0V, Force Current	---	---	-16	A
I _{SM}	Pulsed Source Current ^{2,5}		---	---	-32	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V_{DD}=-25V, V_{GS}=-10V, L=0.1mH, I_{AS}=-20.5A
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

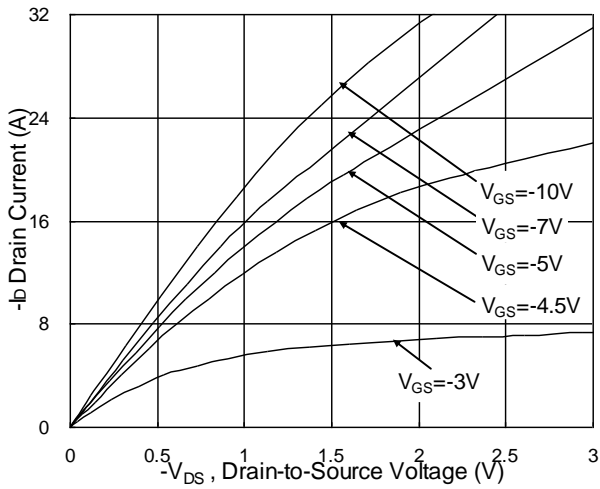


Fig.1 Typical Output Characteristics

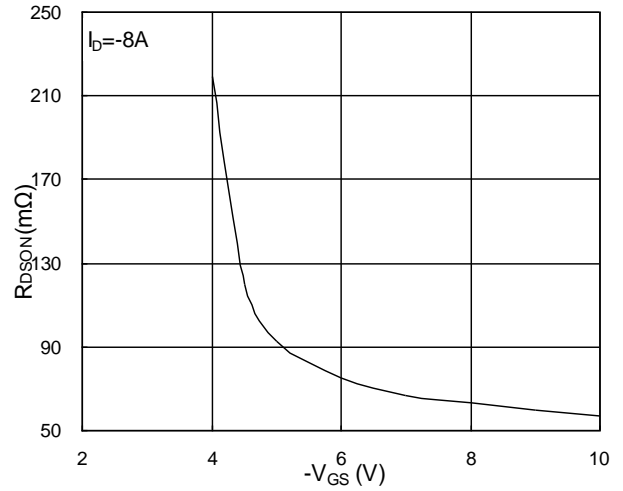


Fig.2 On-Resistance v.s Gate-Source

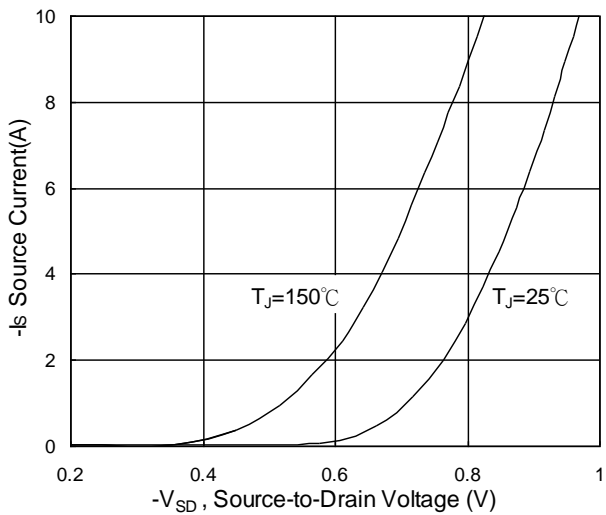


Fig.3 Forward Characteristics Of Reverse

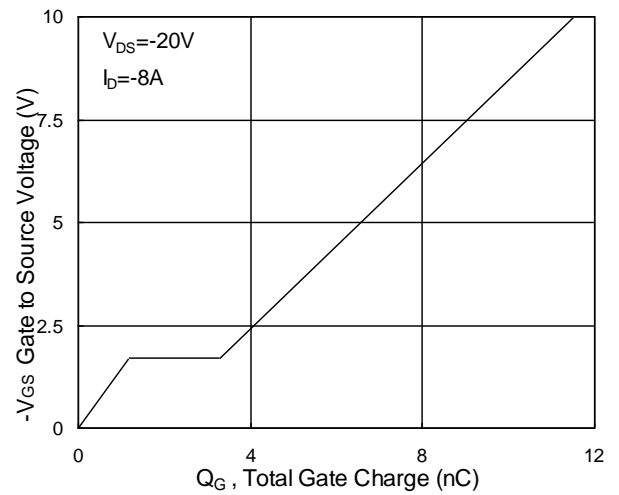


Fig.4 Gate Charge Characteristics

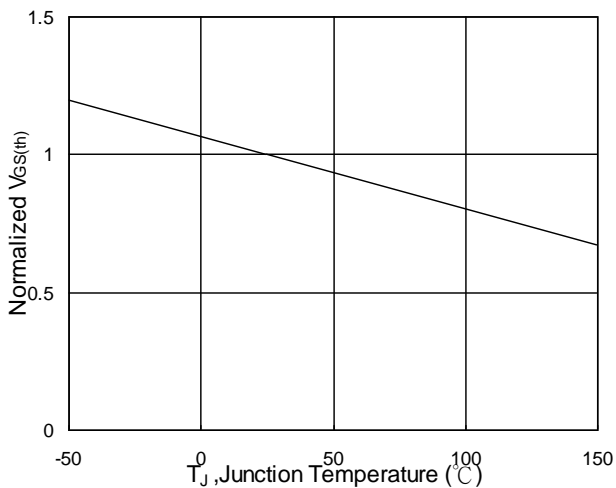


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

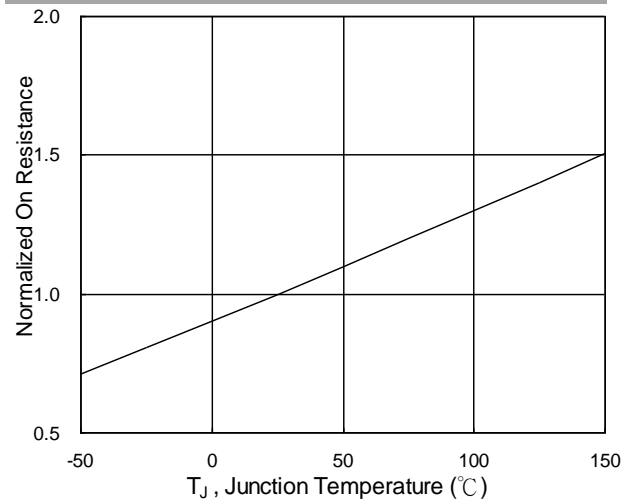


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

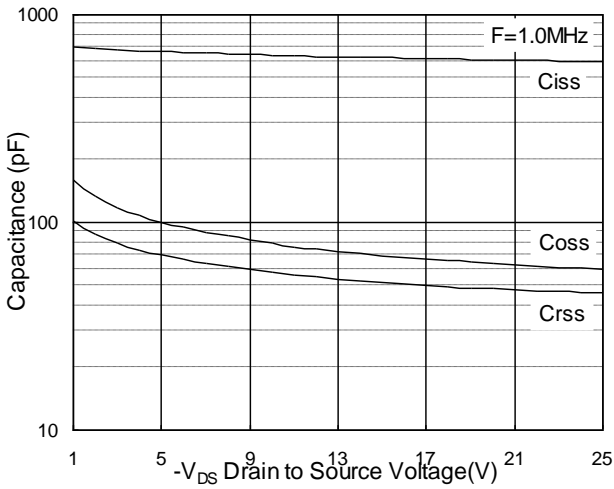


Fig.7 Capacitance

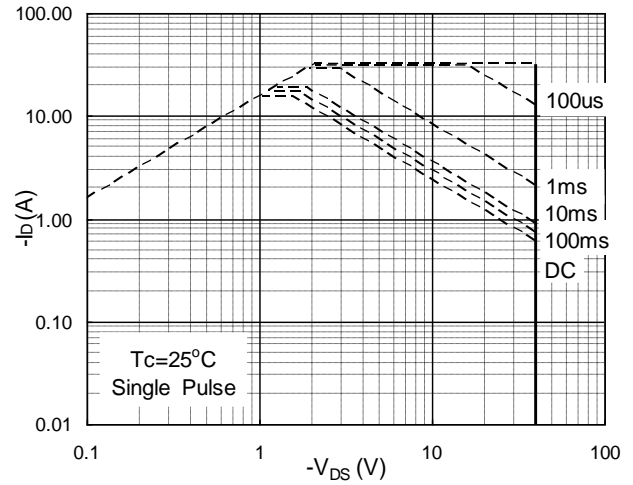


Fig.8 Safe Operating Area

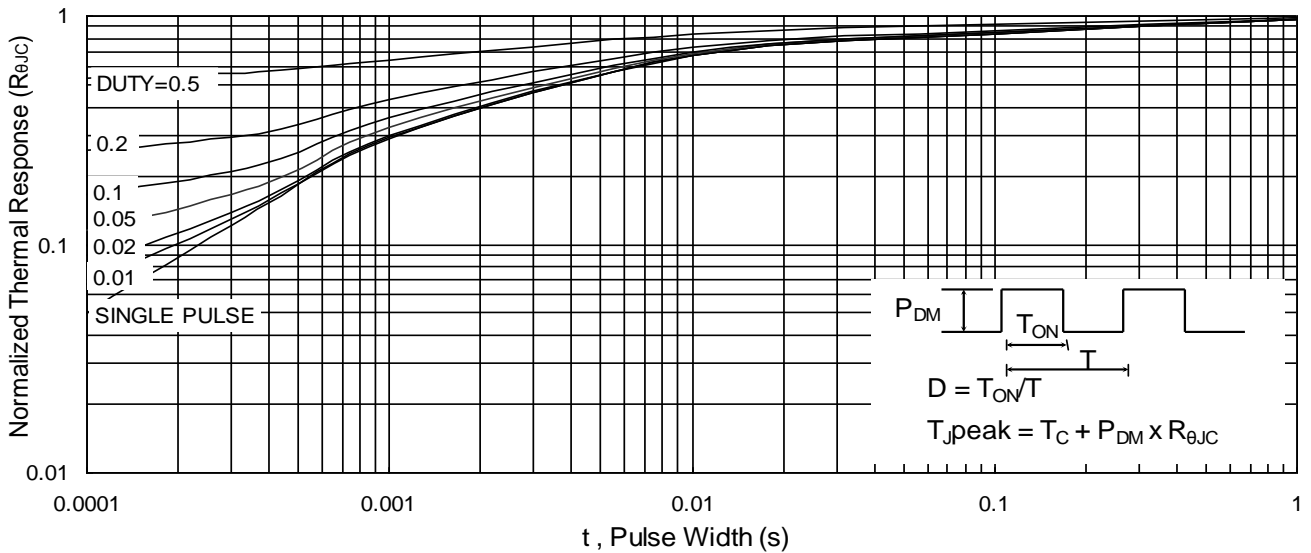


Fig.9 Normalized Maximum Transient Thermal Impedance

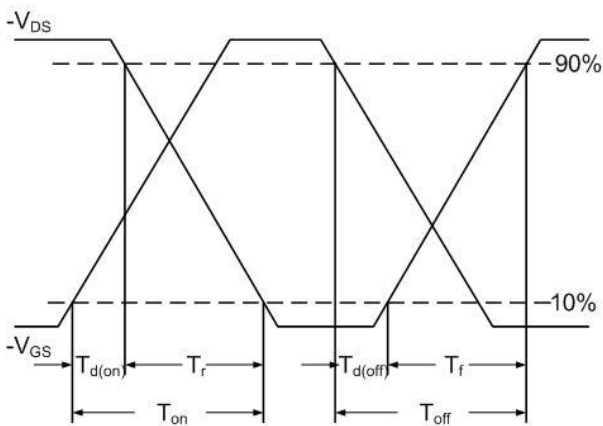


Fig.10 Switching Time Waveform

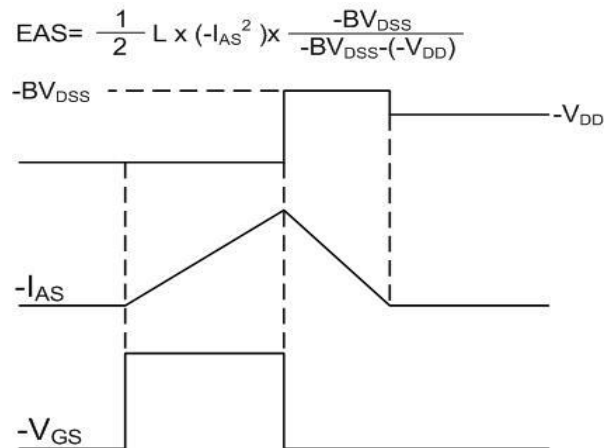


Fig.11 Unclamped Inductive Switching Waveform