

**Features**

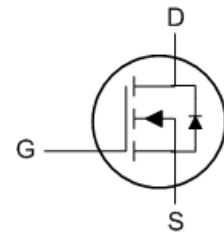
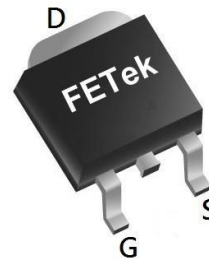
- ★ Advanced Trench Technology
- ★ Low Gate Charge
- ★ 100% EAS Tested
- ★ RoHS and Halogen-Free Compliant

**Applications**

- SMPS Synchronous Rectification
- DC/DC Converters
- Or-ing

**Product Summary**


BVDSS	RDSON	ID
40V	1.9mΩ(Typ.)	100A

**TO252 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	±20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	100	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	82	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	400	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	400	mJ
$I_{AS}$	Avalanche Current	40	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	125	W
$T_{STG}$	Storage Temperature Range	-55 to 150	°C
$T_J$	Operating Junction Temperature Range	-55 to 150	°C

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	50	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	1	°C/W

**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	40	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	1.9	2.4	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	---	2.5	3.6	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.6	2.2	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	---	53	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.0	2.5	Ω
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	---	45	54	nC
Q <sub>g</sub>	Total Gate Charge		---	90	108	
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =15V, V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	12	15	
Q <sub>gd</sub>	Gate-Drain Charge		---	18.5	24	
T <sub>d(on)</sub>	Turn-On Delay Time		---	18.5	23	ns
T <sub>r</sub>	Rise Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω,	---	9	12	
T <sub>d(off)</sub>	Turn-Off Delay Time	I <sub>D</sub> =20A	---	58.5	70	
T <sub>f</sub>	Fall Time		---	32	39	
C <sub>iss</sub>	Input Capacitance		---	3972	4650	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz	---	1119	1310	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	82	105	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	100	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.5mH, I<sub>AS</sub>=40A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 100A.

Typical Characteristics

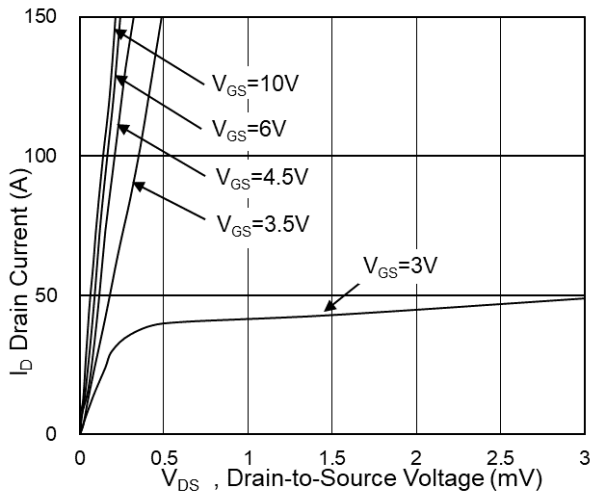


Fig.1 Typical Output Characteristics

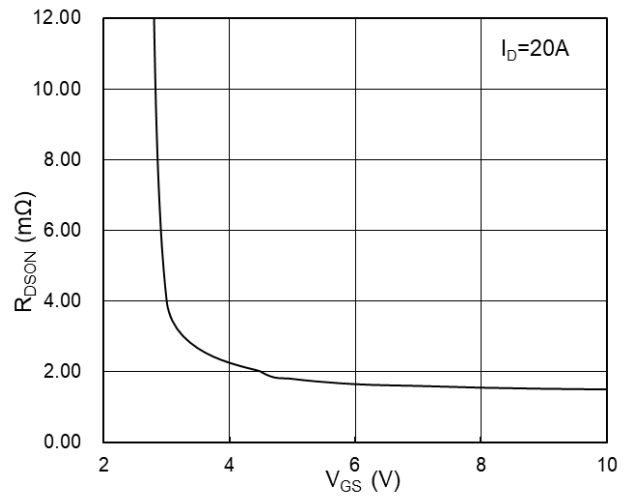


Fig.2 On-Resistance vs G-S Voltage

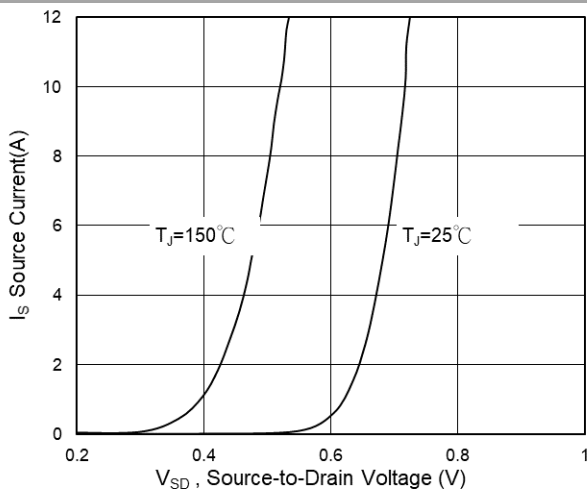


Fig.3 Source Drain Forward Characteristics

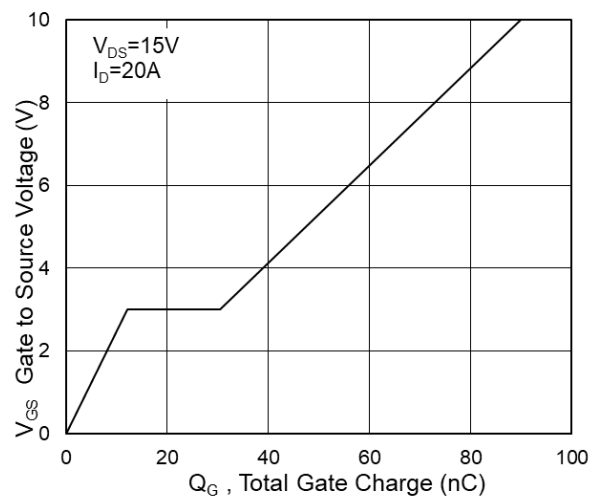


Fig.4 Gate-Charge Characteristics

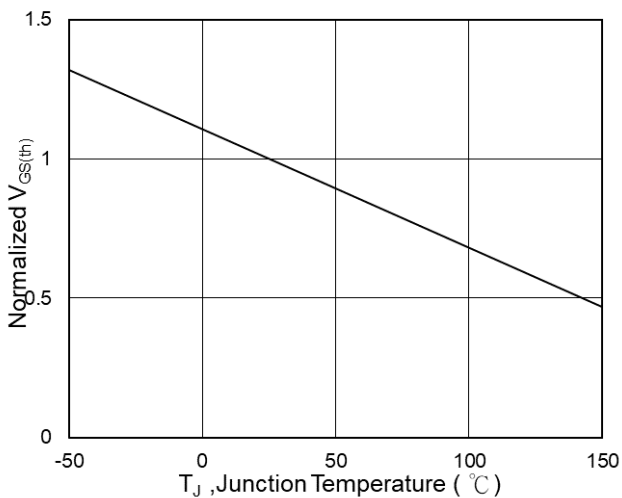


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

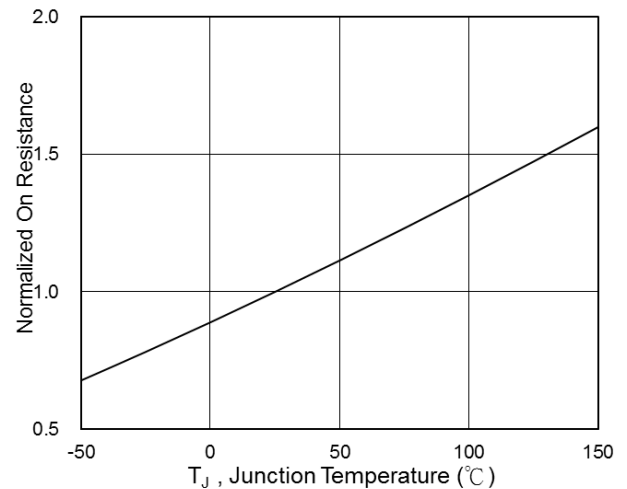


Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$

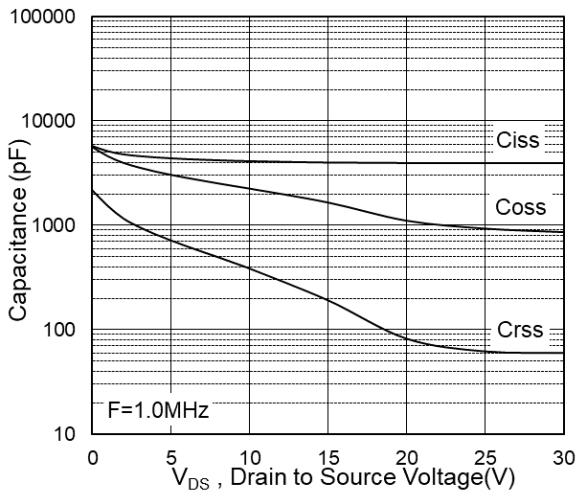


Fig.7 Capacitance

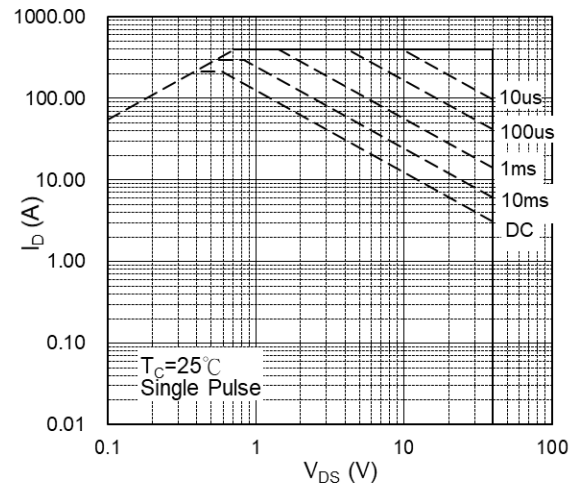


Fig.8 Safe Operating Area

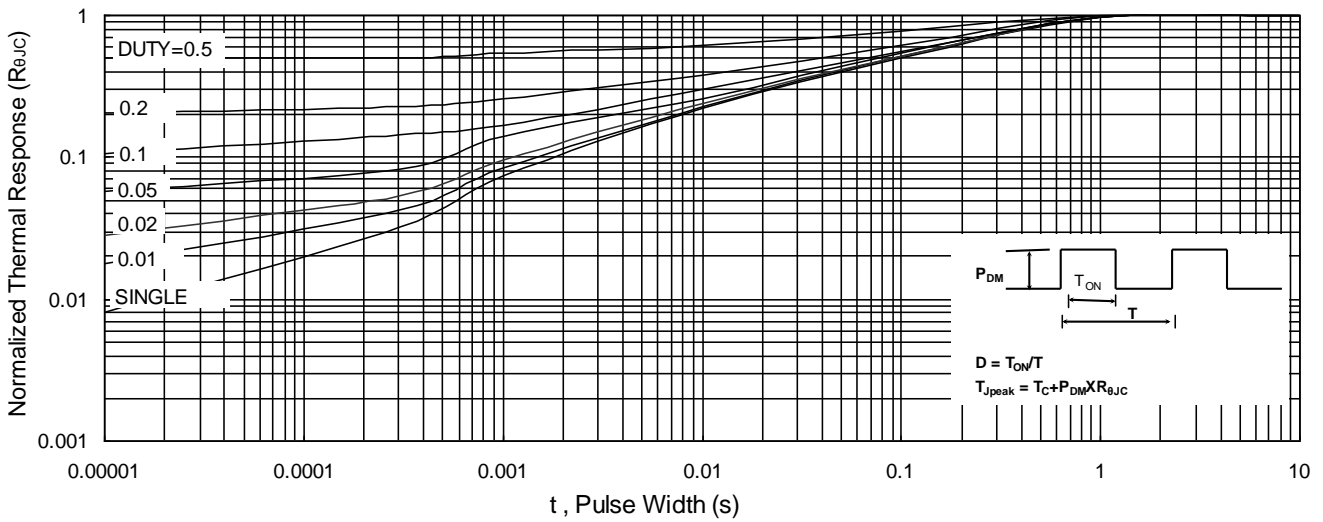


Fig.9 Normalized Maximum Transient Thermal Impedance

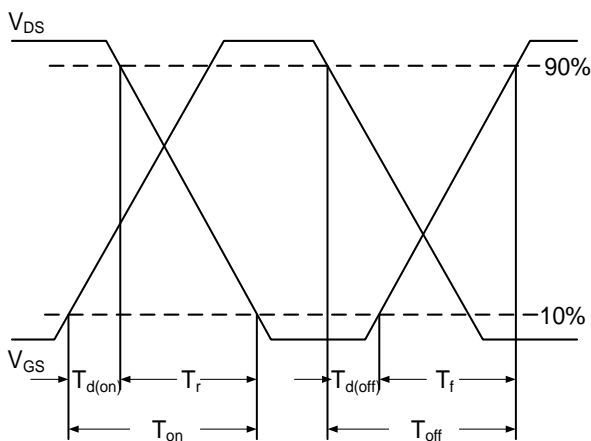


Fig.10 Switching Time Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

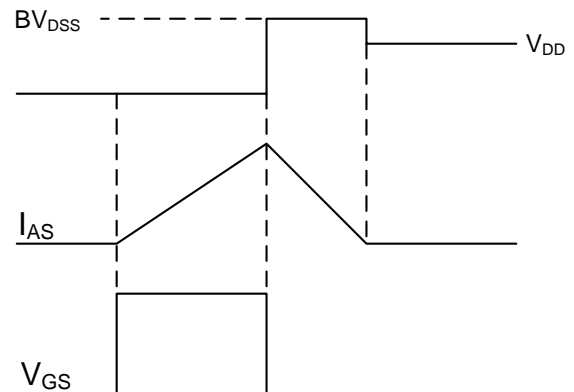


Fig.11 Unclamped Inductive Switching Waveform